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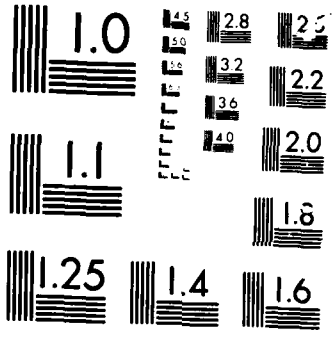

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AD-A169 201

VLSI PROCESS PROBLEM DIAGNOSIS AND YIELD PREDICTION: A COMPREHENSIVE TEST STRUCTURE AND TEST CHIP DESIGN METHODOLOGY

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Abstract

A comprehensive test chip has been designed for fabrication line monitoring, process problem diagnosis, and yield modeling of a two layer metal, oxide isolated, N-well CMOS process. The design philosophy emphasizes global optimization of test structure choices and sizes necessary for sufficiently sensitive detection and unambiguous determination of functional location and densities of process related yield detractors. The test chip has been designed to accompany a microprocessor chip, and will be used to predict its yield. This presentation will describe the salient features of the optimized test structures and the systematic design methodology which emphasizes (i) test structure selection strategy, (ii) test structure sizing, (iii) test chip layout, and (iv) applications to yield prediction based on the elemental defect densities extracted from the defect locator test structures.

Introduction

Integrated circuit yield modeling has been discussed in the published literature for over two decades. Researchers have investigated methods of modeling defect sensitivities in ICs [1], defects in IC lithographic processes [2,3] and defect clustering [4]. Most authors assume mathematical expressions for defect density distributions used in their yield models [5] and some have resorted to computer simulations to substantiate their theories [6]. Regrettably, only a few publications discuss test structures and test chip design, and none of them present a systematic, comprehensive design methodology which could be used to to optimize and enhance existing test structure designs and to design additional structures which combined could provide a comprehensive process problem diagnosis and yield modeling test vehicle.

After careful analysis of the many scattered, narrowly focused reports, we have developed a fresh design philosophy which has guided our design of a comprehensive test chip primarily aimed at unambiguous process problem diagnosis, but also capable of providing the detailed defect density information required for accurate yield prediction of circuits built with a two layer metal, oxide isolated, N-well CMOS process currently used at Stanford's Center for Integrated Systems.

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Test Structure and Test Chip Design Methodology

The objective of our design was to produce a test chip capable of assessing the ability of our process to produce functioning circuits. There are four steps in our approach: 1) develop measurement structures for determination of circuit simulation parameters, 2) develop extensive process decomposition structures to extract elemental metallization and front-end process defect densities, 3) develop composite structures to examine defect superposition, and 4) develop yield prediction models utilizing in-process and end-of- process data and verify model accuracy using composite structures and simple circuits. To implement this approach required a judicious and comprehensive design methodology. Our approach emphasizes (i) test structure selection strategy, (ii) test structure sizing, (iii) test chip layout, and (iv) yield prediction model development strategy.

The most important element of our design is the test structure selection strategy. We decided that a comprehensive evaluation of an IC process required defect monitor structures to evaluate the integrity of bulk, interface, and topographical properties of the technology which could be accomplished with interrelated sets of test structures designed to examine (i) gate oxides, (ii) junctions, (iii) source/drain isolation, (iv) device to device isolation, (v) interconnect isolation, (vi) interconnect continuity, (vii) contact and via continuity, and (viii) parametrics. Included in the criteria was the requirement to emulate, where appropriate, the essential features of the circuits whose yield we would want to predict. This aspect is ignored in most test chip design philosophies.

Equally important was appropriate sizing of the selected structures. We decided that the proper approach is to size the defect monitor structures by an appropriate fraction of the product content of the element in question, rather than by arguable defect density requirements. Each defect monitor structure was designed, therefore, to contain at least 25% of the product content of the element in question. Furthermore, each structure was subdivided into multiple substructures with geometrically ratioed sizes to broaden the range of measurable defect densities.

Proper test chip layout is relatively straightforward, although seldom practiced in industry. Our test chip layout emphasizes modularity and independent testability of each test structure. The 2 by N probe pad approach [7] is used exclusively to maximize area utilization in discrete device parametric modules and large area defect monitor modules.

Our yield prediction model development strategy is straightforward and pragmatic. Yield is a function of all yield detractor densities and their associated product content. The total yield of a chip is the product of the component yields of all yield detractors. We feel that our selection of suitably sized, carefully chosen test structures will allow us to isolate each defect mechanism and quantify its density thereby allowing us to project the yield for product chips by upscaling from the defect monitor areas to the product area. This exercise will first be conducted on a variety of composite structures with well defined topographies of moderate complexity. It will then be followed by similar exercises on very large arrays of ring oscillators, which will also permit us to assess the extent of defect clustering and its impact on our yield models. Successful yield prediction on these structures will be used to guide the design approaches and predict the yield of a variety of VLSI and ULSI circuits under development at the Center for Integrated Systems.

Conclusion

We believe we have developed the most comprehensive, integrated set of end-of-process assessment test structures described in the published literature. The presentation will describe the rationale of our design strategy and test structure choices, and their application to yield problem debugging and development of yield prediction models founded on the empirical determination of the elemental defect densities.

Acknowledgments

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[1] C.H. Stapper, "Modeling of Integrated Circuit Defect Sensitivities", IBM J. Res. Dev., Vol. 27, No. 6, 549-557, Nov. 1983.

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[6] S.M. Hu, "Yield Projection for VLSI and Beyond: II. A Computer Experiment", IEEE (USPS 857-240), No. 69, 8-10, March 1984.

[7] M.G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-Pad Approach", Solid State Tech., 89-94, Oct. 1979.

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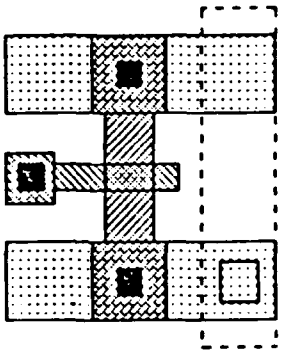
STRUCTURE DESIGN/SELECTION

Orderly Device Decomposition

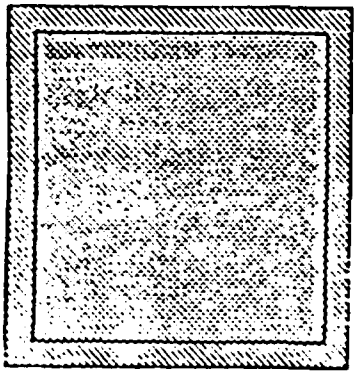


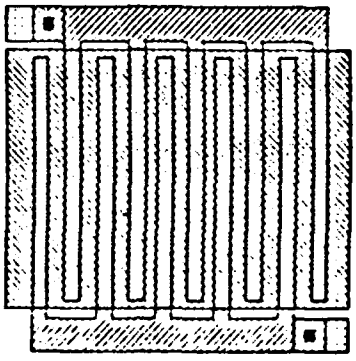
Structures Required:

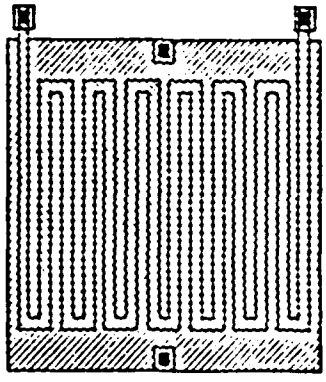
- Gate oxide
- Junctions
- Source-Drain isolation
- Device-Device isolation
- Dielectric integrity
- Interconnect continuity and isolation
- Contact and via continuity
- Parametrics

DECOMPOSITION TEST STRUCTURES

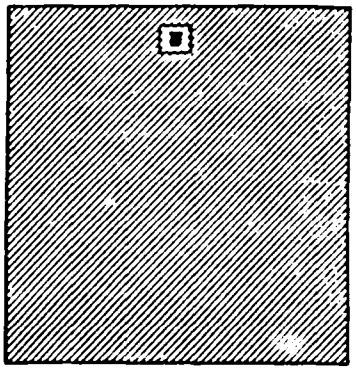
- *Gate Oxide*

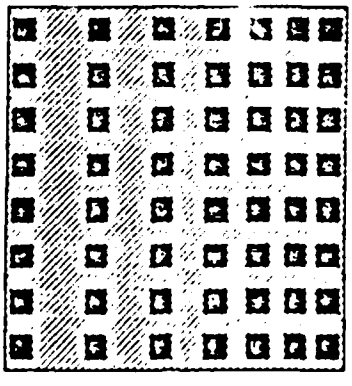


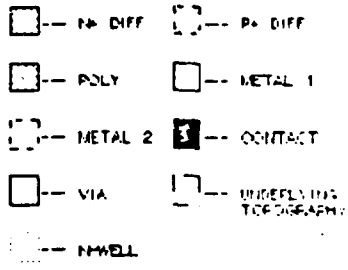




- *Junctions*







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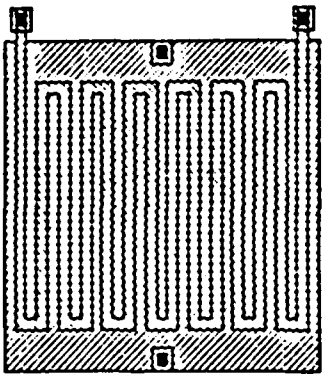
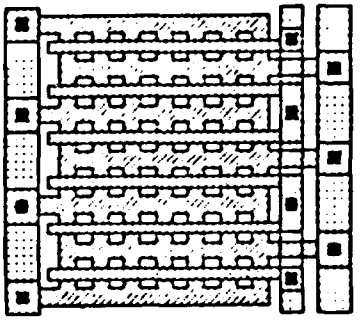
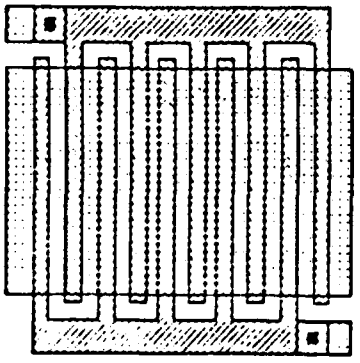
DECOMPOSITION TEST STRUCTURES

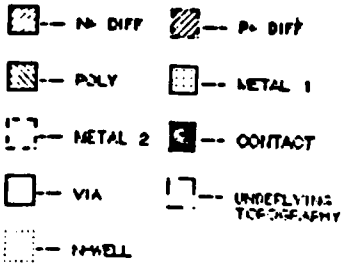
- *Source-Drain Isolation*





- *Device-Device Isolation*





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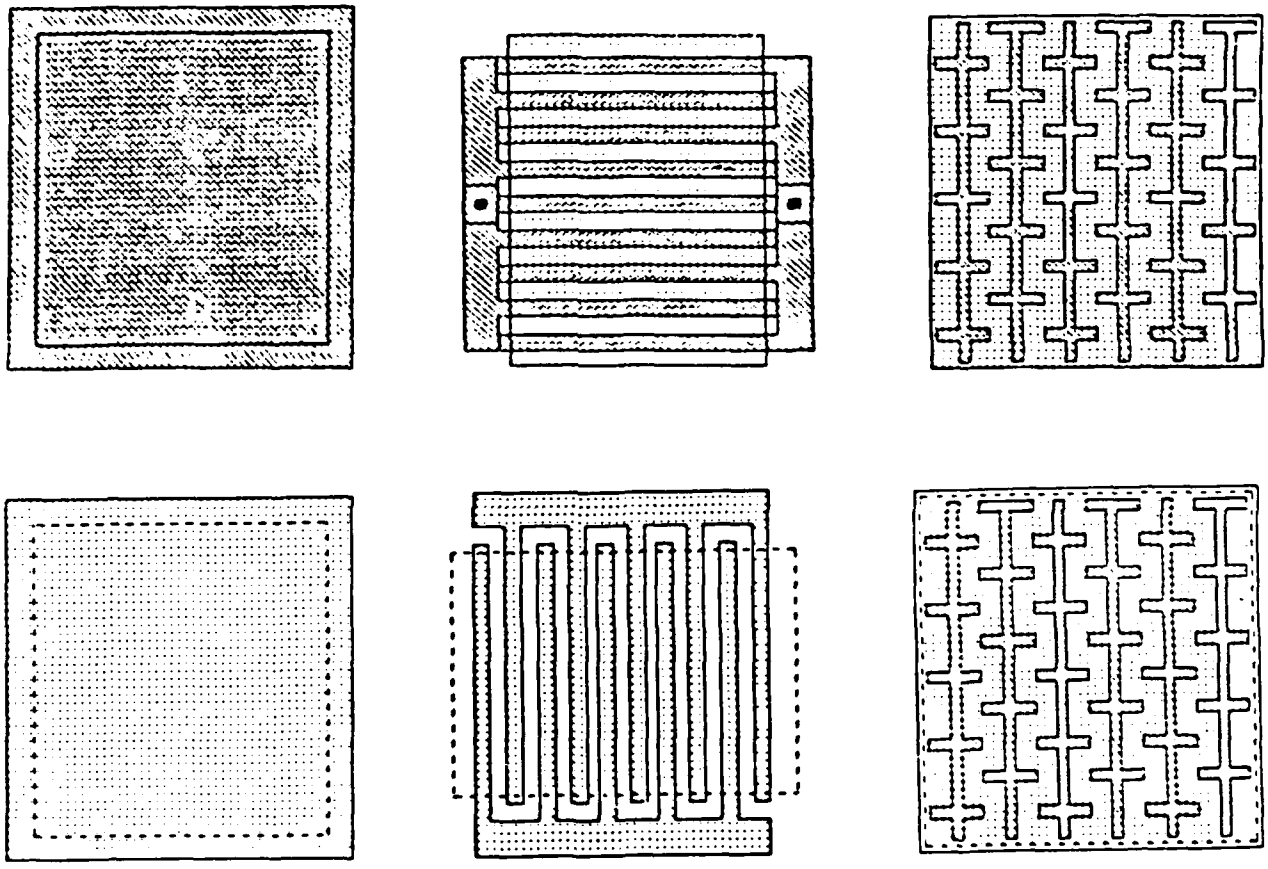
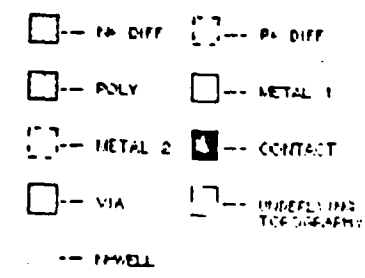
DECOMPOSITION TEST STRUCTURES

- *Dielectric Integrity*





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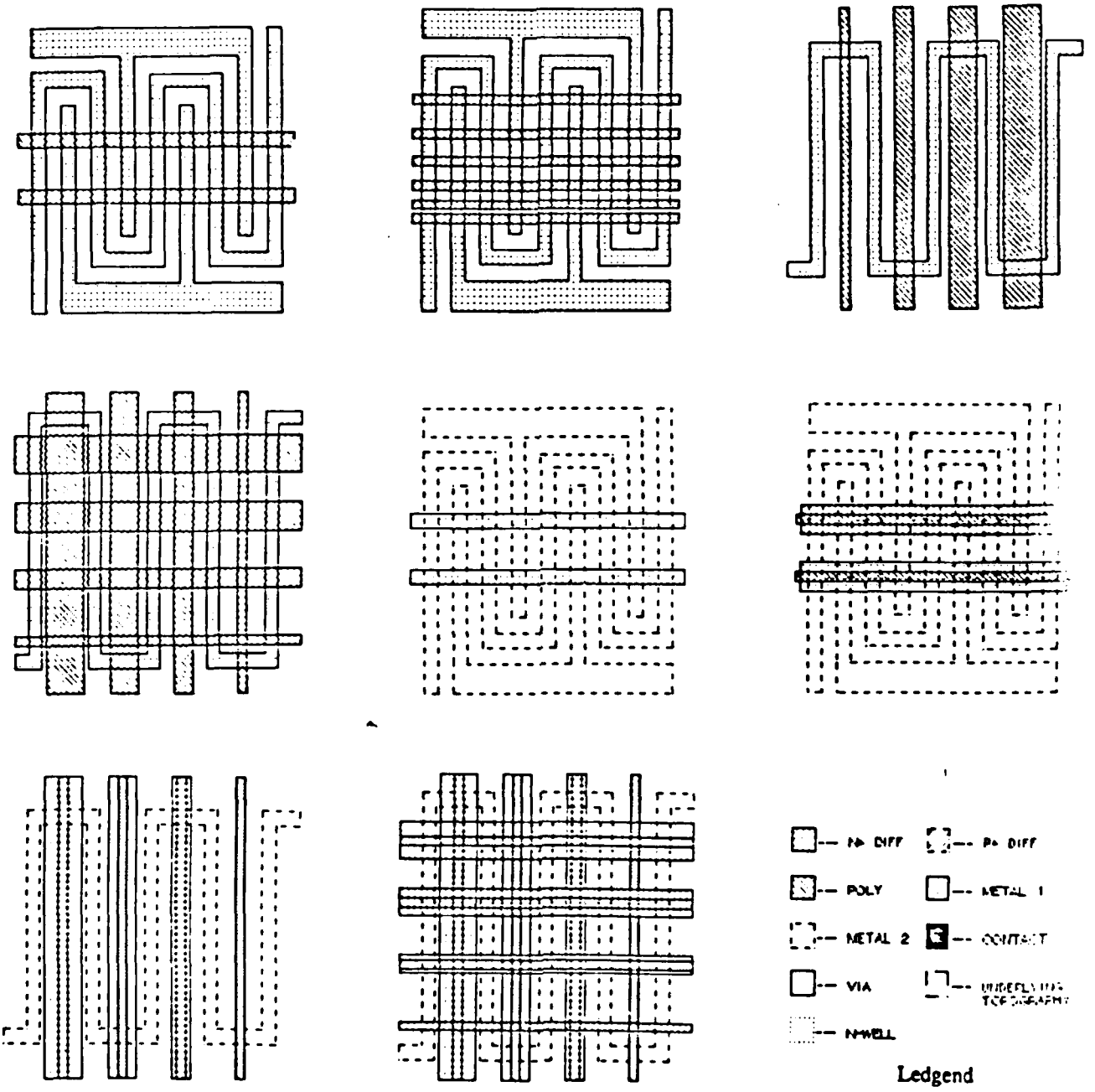
DECOMPOSITION TEST STRUCTURES

- *Interconnect Continuity and Isolation*



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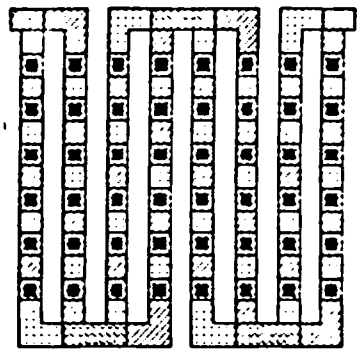
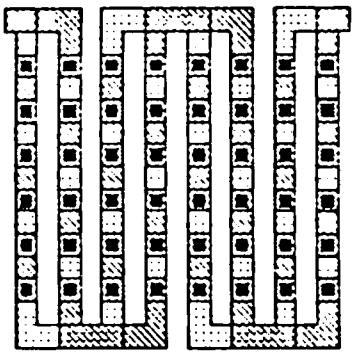
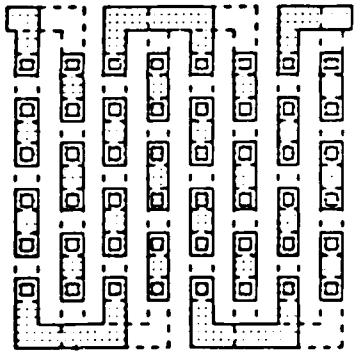
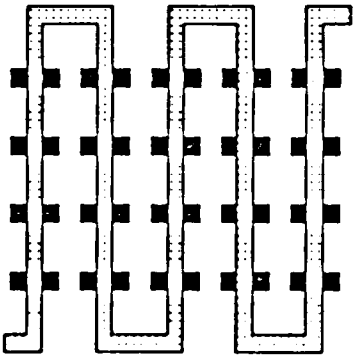
DECOMPOSITION TEST STRUCTURES

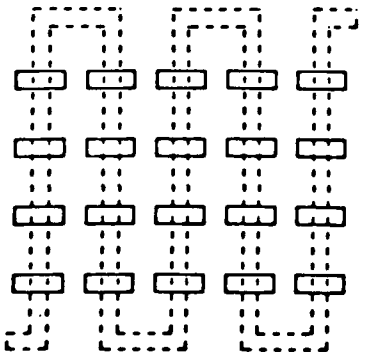
- *Contact and Via Continuity*

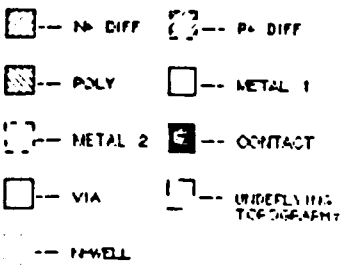












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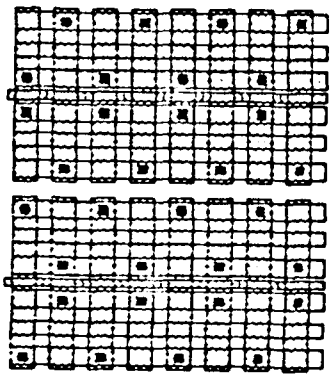
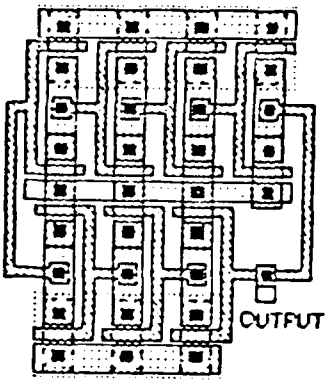
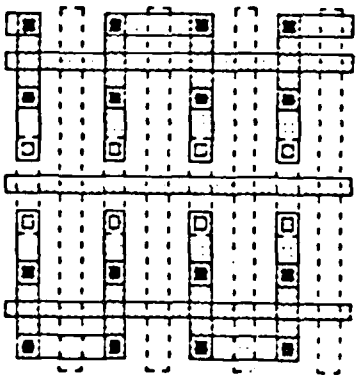
RE-COMPOSITION TEST STRUCTURES

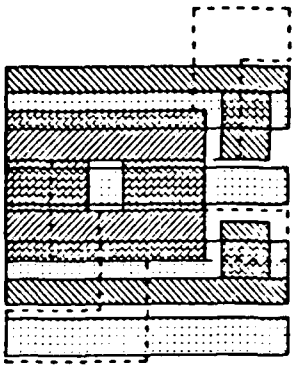
- *Transistor and Ring Oscillator Arrays*

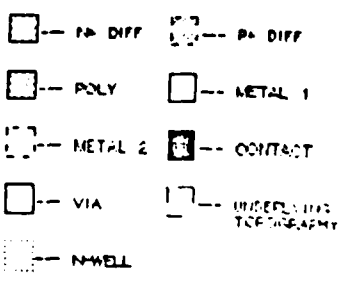




- *Metal 1 and Metal 2*







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TEST CHIP FLOORPLAN

COMPOSITE METALLIZATION (COMB)	COMPOSITE METALLIZATION (SERPENTINE)	COMPOSITE METALLIZATION (COMB)	COMPOSITE METALLIZATION (SERPENTINE)
M2/M1 VIA & COMPOSITE SERPENTINES	N+ DIFF CONTACT SERPENTINES	P+ DIFF CONTACT SERPENTINES	POLY CONTACT SERPENTINES
METALLIZATION LITHOGRAPHY EFFECTS	GATE OXIDE PERIMETER	GATE OXIDE AREA	N+ DIFF JUNCTION
PROCESS PARAMETRICS	SOURCE/DRAIN LEAKAGE & PARAMETRICS	DIFF JUNCTION ISOLATION	P+ DIFF JUNCTION

M1 AREA OVER POLY AREA	M1 AREA OVER POLY CORNERS	M1 AREA OVER POLY LINES	M1 LINES OVER POLY LINES
M2 AREA OVER M1 AREA	M2 AREA OVER M1 AREA OVER POLY CORNERS	M2 AREA OVER M1 LINES	M2 LINES OVER M1 LINES
RING OSCILLATOR ARRAY	RING OSCILLATOR ARRAY	N-CHANNEL TRANSISTOR ARRAY	N-CHANNEL TRANSISTOR ARRAY
RING OSCILLATOR ARRAY	RING OSCILLATOR ARRAY	P-CHANNEL TRANSISTOR ARRAY	P-CHANNEL TRANSISTOR ARRAY

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